CLAIMS

WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a substrate;

a charge storage region on the substrate;

a control gate on the charge storage region; and

a gate mask on the control gate, wherein the gate mask is in the shape of a spacer.

2. A non-volatile semiconductor memory device according to claim 1, further comprising:

a select gate formed on the substrate and a sidewall of the charge storage region; and

a conductive region formed on the substrate adjacent another sidewall of the charge storage region, the charge storage region, the control gate, the gate mask and the select gate forming a first unit cell.

3. A non-volatile semiconductor memory device according to claim 2 further comprising a second unit cell being symmetrical and opposite to the first unit cell, wherein the first unit and the second unit cell share the conductive region.

4. A non-volatile semiconductor memory device according to claim 2, wherein the first unit cell further comprises a LDD spacer on a sidewall of the select gate.

5. A non-volatile semiconductor memory device according to claim 2 further comprising:

a drain formed in the substrate adjacent to the select gate and opposite to the conductive region; and

a bit line electrode electrically connected to the drain.

6. A non-volatile semiconductor memory device according to claim 3 further comprising a source electrode on the conductive region, wherein the source electrode is electrically isolated from the control gate by a source-side spacer.

7. A non-volatile semiconductor memory device according to claim 2, wherein the select gate is in the shape of a spacer.

8. A non-volatile semiconductor memory device according to claim 1, wherein the charge storage region comprises:

a floating gate dielectric layer on the substrate;

a floating gate on the floating gate dielectric layer; and

an inter poly dielectric layer on the floating gate.

9. A non-volatile semiconductor memory device according to claim 1, wherein the charge storage region comprises an ONO layer.

10. A non-volatile semiconductor memory device comprising:

a substrate having a source and a drain;

a channel between the source and the drain;

a charge storage region on the channel;

a control gate on the charge storage region; and

a select gate on the channel and between charge storage region and the drain; the charge storage region, the channel, the drain, the control gate and the select gate forming a first unit cell.

11. A non-volatile semiconductor memory device according to claim 10 further comprising a second unit cell being symmetrical and opposite to the first unit cell, wherein the first unit and the second unit cell share the source.

12. A non-volatile semiconductor memory device according to claim 10, wherein the select gate is in the shape of a spacer.

13. A non-volatile semiconductor memory device according to claim 10 further comprising a gate mask formed on the control gate, wherein the gate mask is in the shape of a spacer.

14. A non-volatile semiconductor memory device according to claim 10 further comprising a LDD spacer on a sidewall of the select gate.

15. A non-volatile semiconductor memory device according to claim 10 further comprising:

a bit line electrode connected to the drain; and

a source electrode on the source, wherein the source electrode is electrically isolated from the control gate by a source-side spacer.

16. A non-volatile semiconductor memory device according to claim 10, wherein the charge storage region comprises:

a floating gate dielectric layer on the substrate;

a floating gate on the floating gate dielectric layer; and

an inter poly dielectric layer on the floating gate.

17. A non-volatile semiconductor memory device according to claim 10, wherein the charge storage region comprises an ONO layer.

18. A method of fabricating a non-volatile semiconductor memory device comprising:

forming a charge storage layer on a substrate;

forming a control gate layer on the charge storage layer;

forming a gate mask in the shape of a spacer on the control gate layer; and

removing the charge storage layer and the control gate layer, wherein the gate mask protects a portion of the charge storage layer and the control gate layer to form a control gate and a charge storage region.

19. The method of claim 18, wherein forming the gate mask comprises:

forming a disposable pattern on the control gate layer;

forming a gate mask layer on the disposable pattern and the control gate layer; and

removing a portion of the gate mask layer to form a gate mask on a sidewall of the disposable pattern.

20. The method of claim 19, wherein removing the charge storage layer and the control gate layer comprises:

etching the charge storage layer and the control gate layer using the gate mask and the disposable pattern as a etching mask thereby protecting a portion of remaining the charge storage layer and the control gate layer under the gate mask and the disposable pattern;

removing the disposable pattern; and

etching the remaining portion of the charge storage layer and the control gate layer using the gate mask as an etching mask thereby forming a control gate and a charge storage region under the gate mask.

21. The method of claim 20 further comprising:

forming a source in the substrate adjacent to a sidewall of the control gate; and

forming a source-side spacer on the sidewalls of the control gate and the charge storage region;

forming a source electrode on the source, wherein the source electrode is isolated from the control gate and the charge storage region by the source side spacer.

22. The method of claim 18 further comprising forming a select gate on a sidewall of the charge storage region.

23. The method of claim 22, wherein the select gate is in the shape of a spacer.

24. The method of claim 22 further comprising:

forming an LDD region in the substrate using the select gate as a LDD implantation mask; and

forming a LDD spacer on a sidewall of the select gate.

25. The method of claim 18, wherein forming the charge storage layer comprises:

forming a floating gate dielectric layer on the substrate;

forming a floating gate layer on the floating gate dielectric layer; and

forming an inter poly dielectric layer on the floating gate layer.

26. The method of claim 18, wherein forming the charge storage layer comprises forming an ONO layer on the substrate.